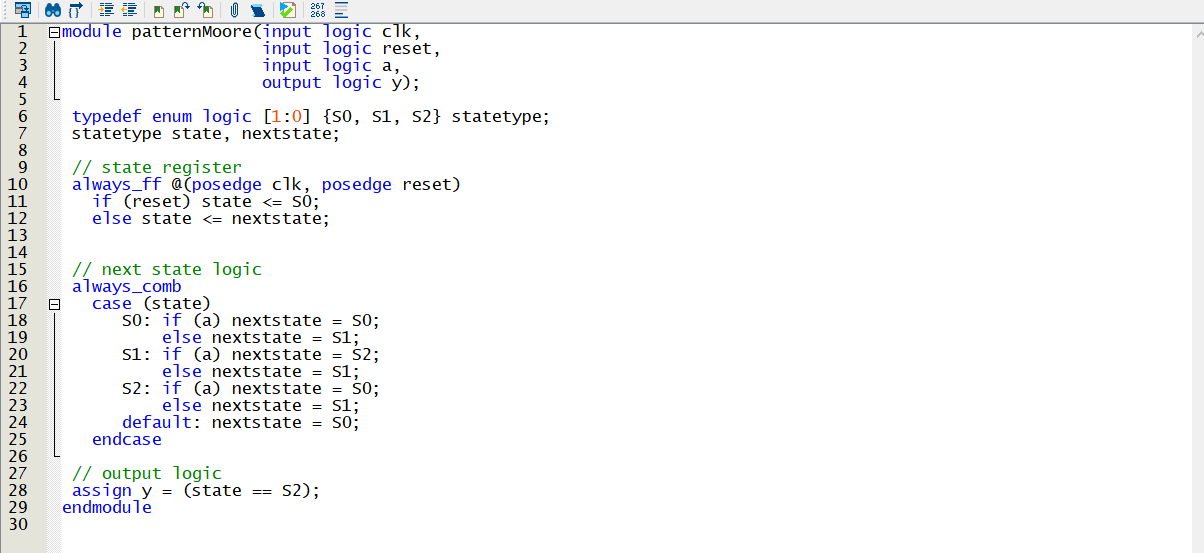
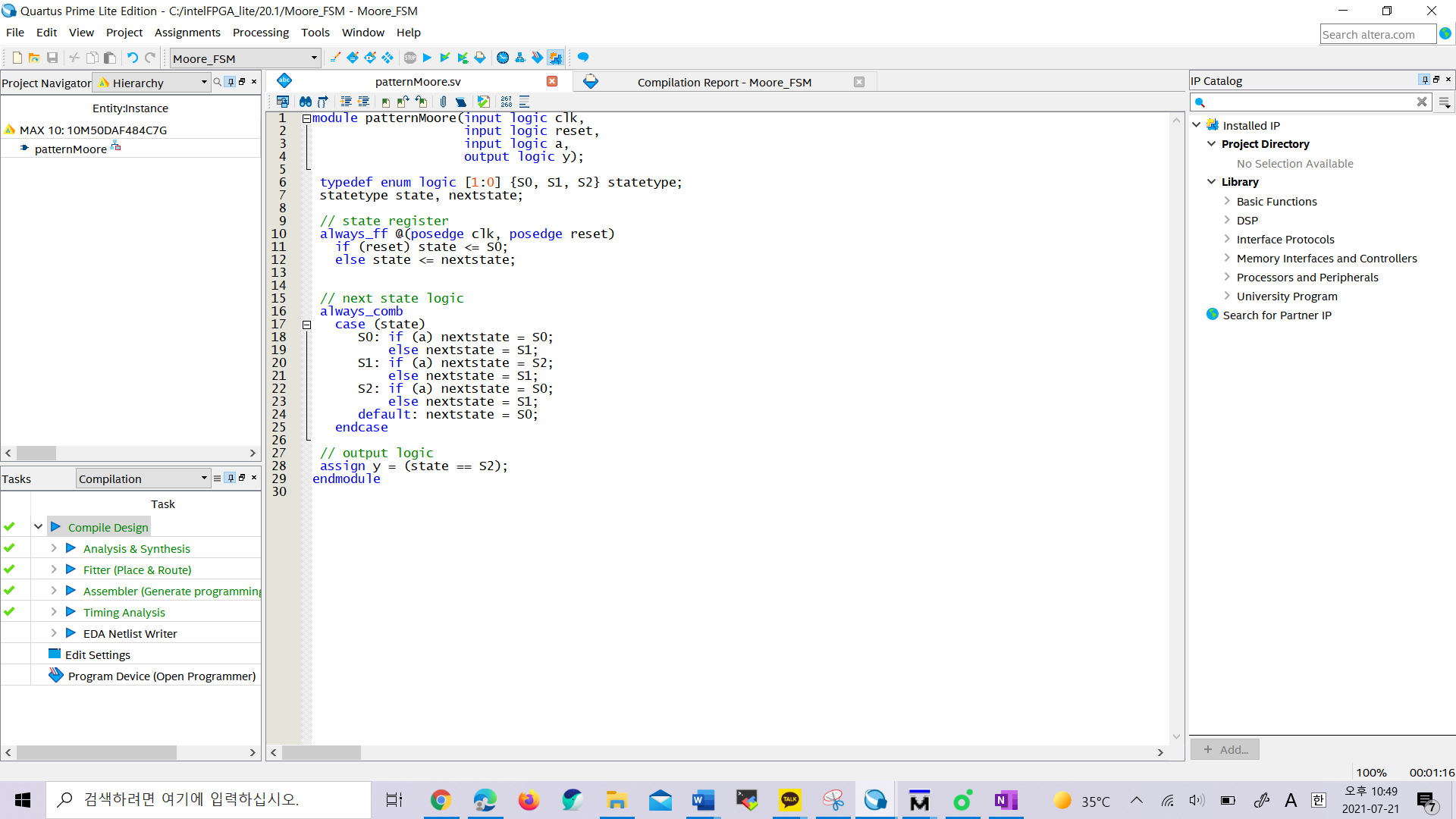
1. HDL source (System Verilog file)





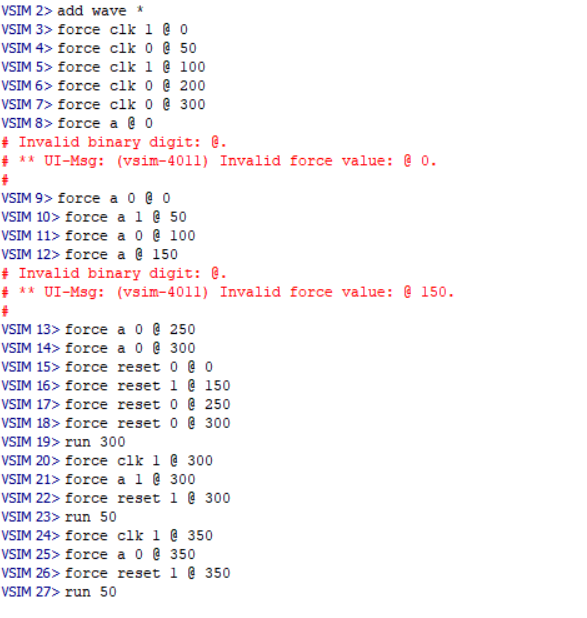
(The System Verilog source is compiled successfully.)

1. Interface definitions

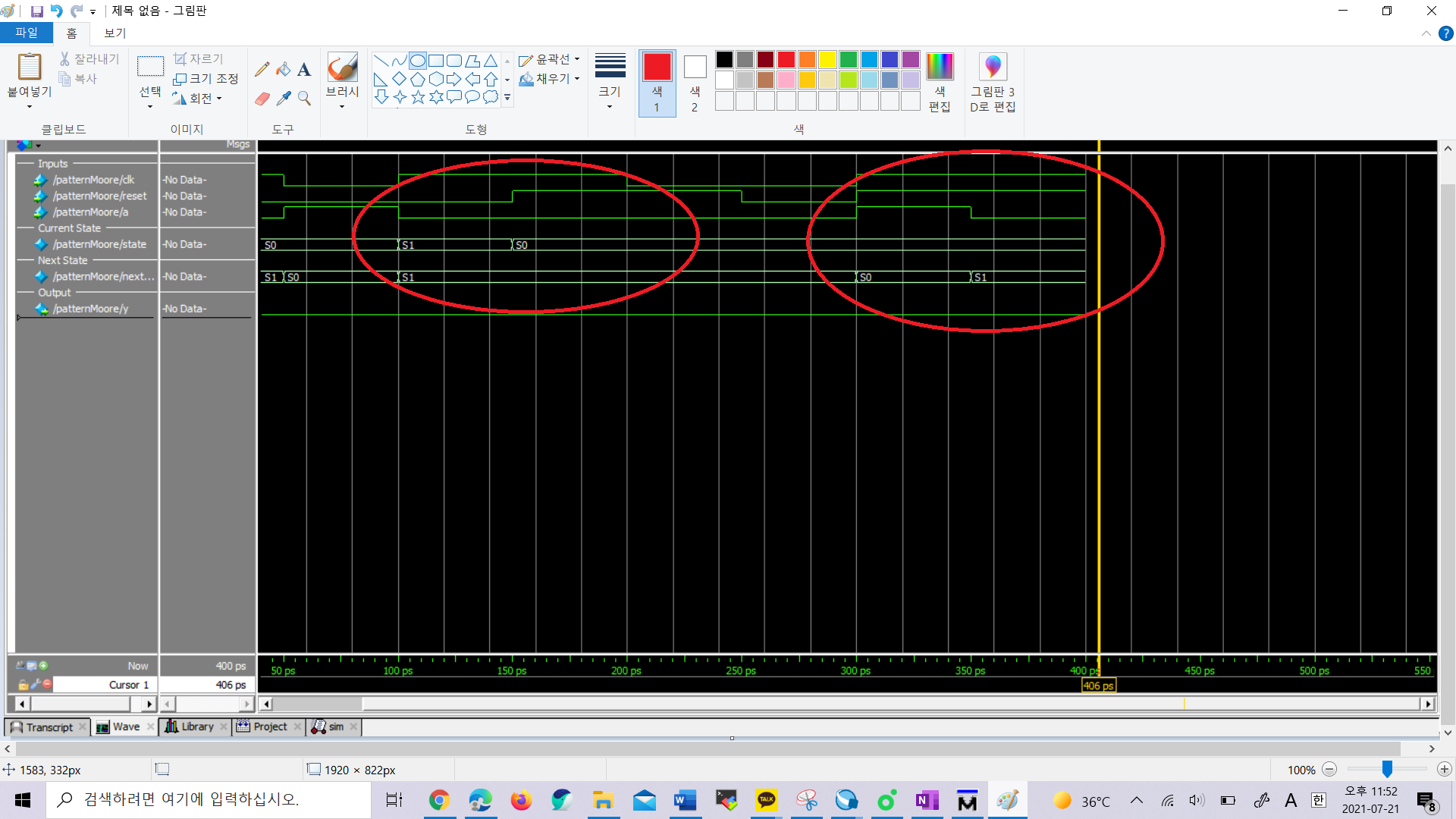
<Expected inputs and results>

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Current State | Input (a) | CLK | Reset | Next State | Output |
| S0 | 0 | 0 | 0 | S1 | 0 |
| S0 | 1 | 0 | 0 | S0 | 0 |
| S0 | 0 | 1 | 0 | S1 | 0 |
| S0 | 1 | 1 | 1 | S0 | 0 |
| S0 | 0 | 0 | 1 | S0 | 0 |
| S0 | 1 | 0 | 0 | S0 | 0 |

1. List of the script



1. Simulation Output



1. System Validation Summary

In the prediction of the left red circle, when the value of reset is 0 and the value of a is 1with current state S1, the next will be S1. However, in the simulation, as the value of reset changes to 1, the actual next state was S0.

In the prediction of the right red circle, when the value of the reset is 1 and the value of a is 0 with current state 0, the next state will be S0. However, in the simulation, the next state was S1.

Thus, the prediction was proved wrong through the simulation.